AMENDMENTS TO THE CLAIMS

Please amend the claims as follows:

1.-15. (Cancelled)

16. (New) A receiver/decoder comprising:

at least one port for receiving messages;

at least one application module;

a memory including a buffer section and a FIFO section;

a buffer controller responsive to a message appearing at the at least one port,

wherein the buffer controller is configured to write the message into the buffer section and, after complete writing of the message, to read the message from the buffer section out to the at least one application module in response to a control signal from the at least one application module; and

a FIFO controller coupled to the at least one port, the memory, and the at least one application module and responsive to a message appearing at the port to which the FIFO controller is coupled,

wherein the FIFO controller is configured to write the message into the FIFO section of the memory, read the message from the FIFO section out to the at least one application module, and read the message from the FIFO section out to a further port without awaiting complete writing of the message;

thereby enabling the receiver/decoder to receive, depending on the needs of an application module or on the nature of the message, a message at the at least one port to be read out to the further port without awaiting complete writing of the message and to be read out to the at least one application module either after complete writing of the message or without awaiting complete writing of the message.

17. (New) The receiver/decoder according to claim 16 wherein the FIFO controller includes an occupancy detector for detecting the state of occupancy of the FIFO section.

18. (New) The receiver/decoder according to claim 17 wherein the occupancy detector is adapted to detect overflow and underflow of the FIFO section.

19. (New) The receiver/decoder according to claim 17 wherein the occupancy detector is adapted to detect at least one threshold of impending overflow and underflow of the FIFO section.

20. (New) The receiver/decoder according to claim 16, wherein the FIFO controller is arranged to flush a message from the FIFO section.

21. (New) The receiver/decoder according to claim 16 wherein the FIFO section comprises a plurality of FIFO buffers and the FIFO controller comprises a respective plurality of FIFO register controllers.

22. (New) The receiver/decoder according to Claim 16, wherein the buffer section comprises two buffers areas defined by respective buffer registers in the buffer controller.

23. (New) The receiver/decoder according to Claim 22 wherein the buffer controller is operable in a bit stream mode in which an incoming bit stream is directed into the currently selected buffer area and is then switched between the two buffer areas as each buffer area in turn becomes full.

24. (New) The receiver/decoder according to Claim 22 wherein the buffer controller is operable in a datagram mode in which the length of an incoming message is compared with the free space in the currently selected buffer area, and if that space is less than the length of the message, the other buffer area is selected.

25. (New) The receiver/decoder according to claim 16 including a video device application unit fed from the FIFO section and feeding a chip unit which is also fed with a video bitstream.

26. (New) A broadcast system comprising a receiver/decoder according to claim 16 and a transmission system for transmitting messages to the receiver/decoder.